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AUS9-1999-0714 US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Fariborz Assaderaghi, et al.

Serial No: 09/964,127

Filed: September 26, 2001

FOR: METHOD FOR PRODUCING AN
INTEGRATED CIRCUIT

Mail Stop Non Fee Amendment

Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Group Art Unit: 2822

Examiner: Jeff Vockrodt

Via Facsimile: 703-872-9318

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RESPONSE TO FIRST OFFICE ACTION

TECHNOLOGY CENTER 2800

This paper is submitted in response to the Office Action mailed March 28, 2003, in the above-identified application, and is filed within the three-month shortened statutory period for response set in the Office Action.

Please amend the application as follows:

1 IN THE DISCLOSURE

- 2 1. Replace the paragraph beginning at page 1, line 5 with the following paragraph:

3 ~~The present application is a divisional of U.S. Patent Application Serial~~
4 No. 09/435,872, filed November 8, 1999, entitled "DECOUPLING CAPACITOR
5 STRUCTURE AND METHOD FOR MAKING AN INTEGRATED CIRCUIT
6 CAPACITOR," now U.S. Patent No. 6,320,237. The Applicants claim
7 priority from this parent application under 35 U.S.C. §120. This parent
8 application is related to the following U.S. Patent Applications:

- 9 (1) Application Serial No. 09/435,867, filed November 8, 1999, entitled "METHOD,
10 APPARATUS, AND PROGRAM PRODUCT FOR LAYING OUT
11 CAPACITORS IN AN INTEGRATED CIRCUIT," and
12 (2) Application Serial No. 09/435,863, filed November 8, 1999, entitled "ON-CHIP
13 DECOUPLING CAPACITOR ARRANGEMENT PROVIDING SHORT
14 CIRCUIT PROTECTION."

15 The disclosure of the parent application and each of these related applications is
16 incorporated herein by this reference.

- 17
18 2. Replace the paragraph beginning at page 10, line 7 with the following paragraph:

19 The fabrication steps for producing bulk capacitor structure 10 illustrated
20 in Figures 1 through 5 includes first implanting N-well structure 15. This step
21 corresponds to the N-well formation step used elsewhere in the chip for various
22 devices, and comprises masking areas other than the desired N-well areas and
23 implanting N-type dopant material by a suitable method. As shown particularly in
24 Figure 2, the device body 17 comprises a portion of this N-well, N⁺ material.

1 Similarly formed N-well material makes up P-type transistor bodies (first type
2 transistor bodies) elsewhere on the chip. In alternate forms of the invention, an
3 additional mask and implantation step may be performed just for the area in which
4 each device body 17 will reside. This additional mask/implant step may be
5 performed either immediately before or after the step of producing the N-wells
6 and comprises implanting further N-type impurities in areas which will form a
7 device body 17. Although this additional mask/implantation step reduces the
8 resistivity of the device body 17 and thereby increases the frequency response of
9 the capacitor structure 10 and allows improved area efficiency, the step represents
10 an additional fabrication step for the chip 11.

11
12 3. Replace the paragraph beginning at page 10, line 22 with the following paragraph:

13 With N-well 15 and device body 17 formed, the fabrication method next
14 includes applying thin dielectric layer 28 and then the material for anode 30.
15 These steps correspond to the steps of applying the gate insulation layer and gate
16 electrode material, respectively, in transistor devices elsewhere on chip 11, and
17 are performed concurrently with those steps. The areas other than the areas of
18 chip 11 where lateral regions 20 and 22, and first end region 24 are to be located,
19 are then masked off and N-type impurities are implanted in the exposed areas to
20 form these regions. This step corresponds to the step of producing the source and
21 drain regions in N-type transistor structures (second type transistor structures) at
22 other locations on chip 11 and is performed concurrently with that step. It will be
23 appreciated that the silicon oxide layer previously deposited over the entire chip
24 surface preferably remains in place during the formation of lateral regions 20 and

1 22, and first end region 24. The N-type impurity may be driven through the thin
2 silicon oxide layer to be implanted in the underlying N-well silicon. However,
3 alternative fabrication arrangements may remove the thin oxide layer or perform
4 other steps at this point such as producing lightly doped regions corresponding the
5 lightly doped drain regions formed in transistor structures on chip 11.

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TO: EXAMINER JEFF VOCKRODT
FROM: RUSSELL D. CULBERTSON
RE: SERIAL NO. 09/964,127
OUR FILE NO.: AUS9-1999-0711-US2 (2470)

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MESSAGE:

RE: SERIAL NO. 09/964,126
GROUP ART UNIT: 2822

JUN 19 2003
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RESPONSE TO OFFICE ACTION MAILED MARCH 28, 2003

**PLEASE DELIVER IMMEDIATELY TO
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Thank you!

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